Ambarish Vyas

850 N Randolph St. Appt# 1121, Arlington, Virginia, 22203
Ph# 571-314-5992 ♦E-mail: avyas2@masonlive.gmu.edu

EDUCATION

Master of Science in Computer Engineering — **August 2010- Present**
George Mason University, Fairfax.

Master of Science in Computer Engineering — **August 2009- May 2010**
University Of Maryland, Baltimore County.

Bachelor of Engineering in Electronics and Telecommunication Engineering — **August 2005- May 2009**
University Of Pune.

TECHNICAL SKILLS

PROGRAMMING:	C, Microprocessor assembly language.
HDLs:	Verilog, VHDL.
SYSTEMS:	Windows XP/Vista, Mac Snow Leopard, Linux.
TOOLS:	NCSIM, Xilinx, Quartus II, Allegro, Kiel, Cadence Virtuoso, Encounter, Lab-view, Synopsys ASIC tools.
OTHER SOFTWARE:	Net Beans, Microsoft Office.
RELEVANT COURSES:	Advanced VLSI design, VLSI Design Verification and Test, High Speed Digital Design, Advanced Computer Architecture, Computer Arithmetic Algorithms and Implementations, Cryptography and Computer Network Security, ASIC Design, Digital System Design with VHDL.

WORK EXPERIENCE

Teaching Assistant (ECE 448 FPGA & ASIC Design with VHDL) — **January 2011-Present**
George Mason University, Fairfax

- Organize weekly labs involving implementation of Digital Circuits using VHDL.
- Assist students in getting familiar with VHDL coding and FPGA Spartan 3E board.
- Prepare background information and detailed instructions for lab preparation.
- Tutor students on weekly basis to help in ongoing course work and assignments.
- Responsible for grading the labs and course assignments.

Teaching Assistant (CMPE212 Principles of Digital Design) — **September 2009-May 2010**
University of Maryland, Baltimore County

- Organized weekly labs involving implementation of Verilog test bench.
- Assisted students in getting familiar with Verilog coding and lab equipment.
- Prepared background information and detailed instructions for lab preparation.
- Tutored and assisted students on weekly basis to help in ongoing course work and assignments.
- Responsible for grading the labs and course assignments and project.
- Organized pre-examination review lectures and one-on-one help session to assist students.

RELEVANT ACADEMIC WORK

Digital Design with VHDL **August 2010-December 2010**
Folded Architecture- ECHO 512

- Designed and simulated SHA-3 round 2 finalist ECHO-512 bit variant.
- Designed three different architectures, which includes two folded for area optimization and one using embedded resources for FPGA for better throughput/area ratio.

ASIC Design **August 2010-December 2010**
ECHO-512 in ASIC

- Front and Back end design of SHA-3 round 2 finalist ECHO-512 nit variant.
- Performed Synthesis, Area optimization, Functionality check, Static timing analysis, and Floorplanning.

Cryptography and Network Security **August 2010-December 2010**
Generic Padding Circuit

- Designed and simulated a Generic padding circuit for all 14 SHA-3 candidates.
- With minimum area overhead and meeting speed constraints.

High Speed Digital Design **January 2010-May 2010**
Data Acquisition System

- Developed a two-layer PCB to convert analog signal to digital bits to be stored in Data Flash using an 8051 Micro-Controller. And then Playback using a speaker. Keyboard and LCD used to control.
- Implemented the PCB using a combination of amplifiers, 12-bit ADC, capacitors and registers on Allegro.
- Built a 2-layer PCB for measuring capacitance and inductance, and display the result using Lab-view.
- Developing Lab-view program to acquire data bits sent to computer via FPGA for analysis and displays it as a waveform.

Advanced VLSI design **January 2010-May 2010**
Cache Design

- Designed a 2-way Set Associative cache of 128 bytes with TLB.
- Using SRAM and CAM cells for cache and TLB implementation with LRU replacement policy.
- Implemented transistor level schematics and layouts of the Cache and TLB using Virtuoso by Cadence
- Implemented a 4 bit ALU using VHDL. Designed corresponding layouts of the ALU circuit and performed LVS checks against schematics.
- Created standard cell layout for D flip-flop and evaluated out Setup/Hold times through simulations.

Advanced Computer Architecture **August 2009-December 2009**
MIPS Simulator

- Developed a simulator in C for analyzing MIPS architecture CPU employing multi-cycle pipeline.
- Implemented distinct ALU units for Integer Arithmetic and Floating point Arithmetic.
- Created instruction set for data transfer, arithmetic, logical and conditional/branching operations.
- Created benchmarks to verify execution of the simulator and compared it against golden result.

VLSI Design Verification and Test **August 2009-December 2009**
UART Core Test Vectors

- Generated layouts for UART core, one without scan chains with pads and one with full scan and boundary scan using Cadence First Encounter.
- Inserted full and boundary scan chains using RTL compiler**.** Simulated ATPG vectors using Encounter.

Final Year Capstone Design Project **July 2008-April 2009**
Portable ISP Programmer

- Designed and implemented Portable ISP Programmer for programming Philips NXP microcontrollers.
- Designed the peripheral circuit to interface with the Philips microcontroller using Orcad and implemented it into a PCB
- Developed and tested assembly code for communication with serial port using Keil microvision 3.
- Interfaced serial Memory and RTC using I2C protocol.
- 20X4 LCD and 4X4 keyboard was interfaced with the Philips 89v51 controller.

Third Year Innovative Design Project **July 2007-April 2008**
GSM Display System

- Developed a wireless display system using GSM modem to remotely change multiple time-controlled notices.
- Implemented firmware code in assembly for Atmel 89s51 to interface with 16X2 LCD, RTC and Serial memory.
- Used AT commands to talk with GSM modem and get data, which was further sent to display via 89s51 microprocessor interface.